ASP-DCD-00
Differential Clock Divider User Manual

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Product Overview

The ASP-DCD-00 board is a high impedance input clock divider/buffer circuit. It is designed to provide minimum load to a clock source for frequency measurement. Low frequency clocks can be measured with the analog output while higher frequencies, above 2 MHz, can be divided from 2 to 256 times depending on shunt jumper selections. It will accept single ended (Unbalanced) or differential (Balanced) signals with amplitudes as little as 100mV rms. The board requires 5VDC 100mA power source to operate. The output is capable of driving 3.3v TTL logic levels.

Relay disconnects allows the tester channels to be disconnected while the frequency measurements are performed. Connections of the divider circuit is controlled by a tester channel (logic high) or by a jumper on J1.

Hardware Connections

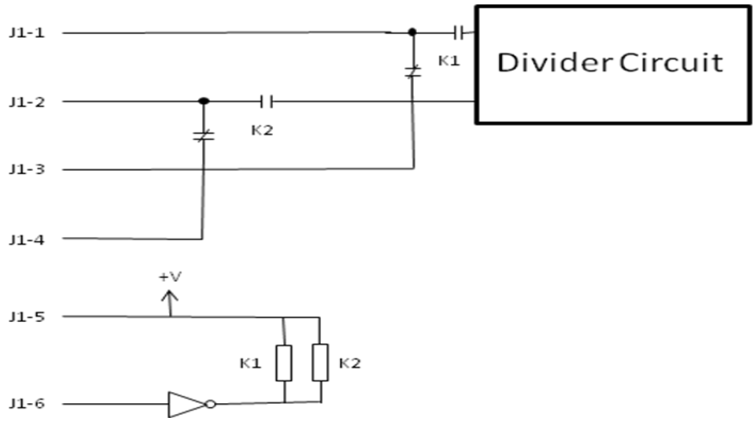
There are 4 connectors on the board as listed below.

Connector	Purpose
J1	Signal Inputs and relay control
J2	5V Power input
J3	Clock Division select and output enable
J4	Divided Signal and Analog outputs

Pin Definitions for Connector J1

1 Non-inverting input. Use twisted pair with pin 2.
2 Inverting input. Use twisted pair with pin 1. Connect to GND for single ended.
3 Connects to pin 1 through the on board relay (Normally closed Contact).
4 Connects to pin 2 through the on board relay (Normally closed Contact).
5 Logic Hi signal which can be used to enable the on board relay.
6 On board relay K1 control. Connect to pin 5 or drive to a logic high.

J1 Circuit Equivalent:



The UUT is accessible via connections J1 pins 1 and 2. Tester channels are connected to J1 pins 3 and 4. Normally closed relay contacts (disconnect relay) connect J1 pin 1 to J1 pin 3 and J1 pin 2 to J1 pin 4. This allows the tester access to the UUT when the disconnect relay is not energized on the Differential Clock Divider Board (DCDB).

A jumper installed between J1 pins 5 and 6 or a logic high applied to J1 pin 6 while power is on the DCDB energizes the disconnect relay. Once the disconnect relay is energized the tester channels are disconnected and the divider circuit is connected. This is the preferred condition for measuring the frequency on the UUT.

Pin Definitions for Connector J2

1 5V DC Power
2 GND

Pin Definitions for Connector J3

1 Select 0
2 GND
3 Select 1
4 GND
5 Select 2
6 GND
7 Output Enable (Active Low)
8 GND

Setting the clock division

The following table lists the clock divisions selectable using the select lines on J3. A Shunt jumper is used to ground the select pins (Logic 0). An on-board pull up resistor will hold the select lines at logic 1 if the pin is left open.

Select 0	Select 1	Select 2	Clock Division
GND	**GND**	**GND**	Divide By 2
Open	**GND**	**GND**	Divide By 4
GND	Open	**GND**	Divide By 8
Open	Open	**GND**	Divide By 16
GND	**GND**	Open	Divide By 32
Open	**GND**	Open	Divide By 64
GND	Open	Open	Divide By 128
Open	Open	Open	Divide By 256

Note: Before the output will be driven the enable pin, J3-7 must be set to logic 0 or grounded.

Pin Definitions for Connector J4

1 Divided clock signal
2 GND
3 Analog Output
4 GND

Appendix A: Hardware Specifications

Model part number: ASP-DCD-00 rev A.2

Input frequency: 10 KHz – 150 MHz

Input impedance: 100 KOhm

Input Voltage: 100mv RMS (280mv PK – PK) to 1.16v RMS (3.3v PK – PK)

Output Impedance: 100 Ohm

Output Voltage: 3.3V TTL

Power supply voltage: 4.85 – 5.15 V

Power supply current: 100 mA (Max)

Clock divider divisions: ÷2, ÷4, ÷8, ÷16, ÷32, ÷64, ÷128, ÷256

Physical dimension: 3” x 0.75” (7.6 cm x 1.9 cm)