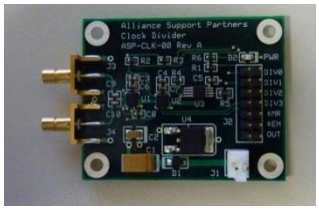
Alliance Support Partners, Inc.

ASP-CLK-00
2.5GHz Clock Divider User Manual

Revision: 1.0, October 28, 2011, Alliance Support Partners, Inc.

Product Overview

The ASP-CLK-00 Clock Divider is designed to divide high frequency signals, up to 2.5GHz, from 4 to 256 times. It will accept single ended (Unbalanced) or differential (Balanced) signals with amplitudes as little as 100mV rms.



The clock division is controlled by 4 shunt jumpers. The circuit can be disabled and the divide by counter reset with 2 control signals. The on board regulator will accept voltages from 4.85 to 15.0V. The output is capable of driving 700mV Peak to Peak into 50 Ohms.

Hardware Connections

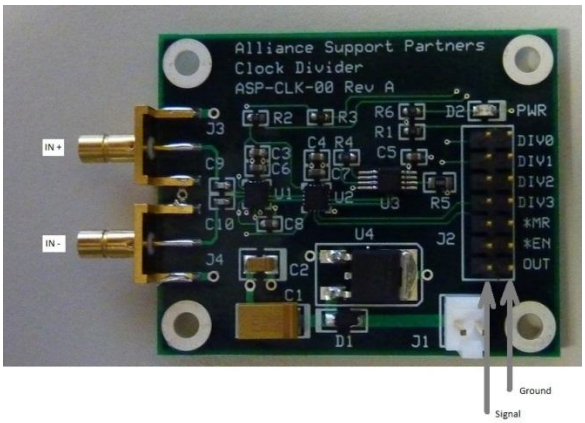
There are 4 connectors on the clock divider board as listed below.

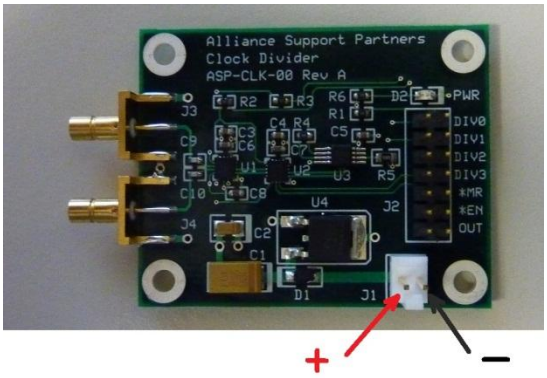
Connector	Purpose
J1	Power input for clock board (4.85 to 15V)
J2	Jumper blocks to set division, and connection for control signals
J3	Non-inverting clock input
J4	Inverting clock input

The clock inputs are SMB Jack card edge connectors. Connect single ended clock signals to J3 and leave J4 open (Unconnected). Differential clock signals are connected to J3 (Non-Inverting) and J4 (Inverting).

Voltages in the range of 4.85 to 15.0V applied to J1 will be regulated to 3.3V by the on board voltage regulator. The polarity of the power connector is pictured below.

The *MR, *EN and OUT signals on J2 are paired with a ground pin to make twisted pair connections easier.





Setting the clock division

The following table lists the clock divisions selectable with 4 shunt jumpers. The 'X' indicates that the shunt jumper is installed.

DIV 3	DIV 2	DIV 1	DIV 0	Clock Division
				Divide by 4
			X	Divide by 8
		X		Divide by 16
		X	X	Divide by 32
	X	X	X	Divide by 64
X		X	X	Divide by 128
X	X	X	X	Divide by 256

Control Signals

There are 2 control signals, *MR and *EN that can be used to control the Clock Divider. These control signals only need to be connected if you plan to use them, otherwise they will be pulled to a level for normal operation. The following table lists their function:

*EN	*MR	Function
X	0	Divide by counters will be set to 0
0	1	Normal operation
1	1	Clock input will be disabled.

Appendix A: Hardware Specifications

Model part number: ASP-CLK-01 rev A

Input frequency: 10 MHz – 2.5 GHz

Input impedance: 50 Ohm

Input Voltage: 100mv RMS (280mv PK – PK) to 1.16v RMS (3.3v PK – PK)

Output Impedance: 50 Ohm

Output Voltage: 700mv PK–PK (Into 50 OHMS) or 1.4v PK-PK (Into IM)

Power supply voltage: 4.85 – 15.0 V

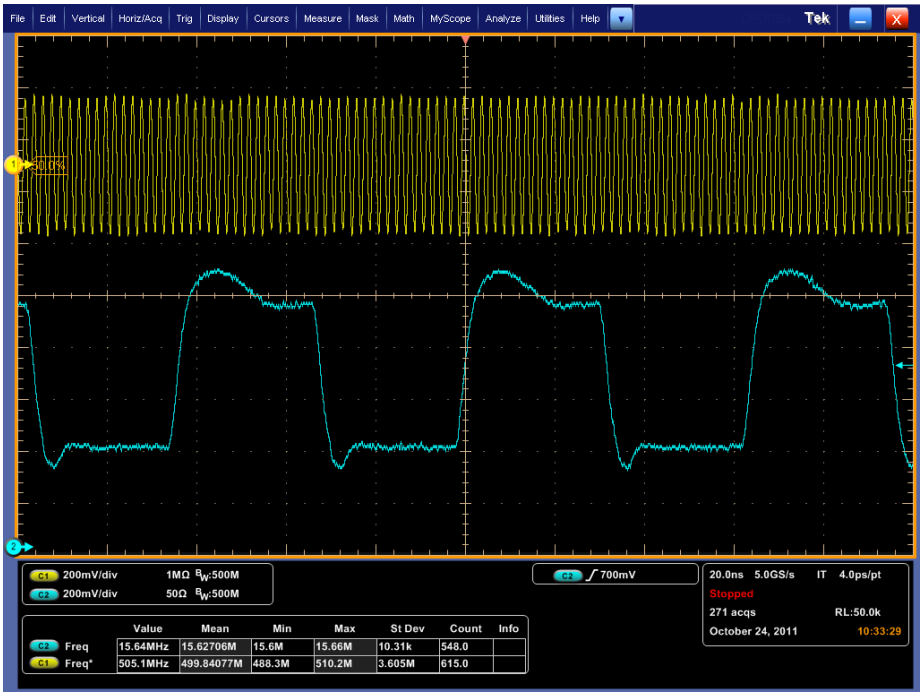
Power supply current: 110 mA

Clock divider divisions: ÷4, ÷8, ÷16, ÷32, ÷64, ÷128, ÷256

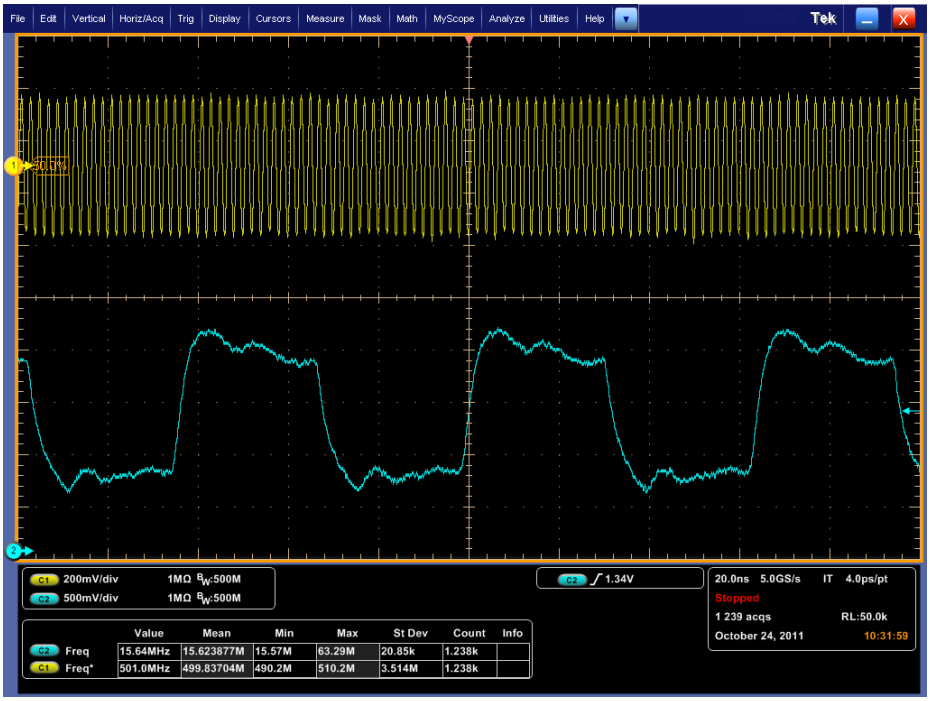
Physical dimension: 2” x 1.6” (5.08 cm x 4.06 cm)

Appendix B – Example Waveforms

Channel 1 = 500 MHz clock Channel 2 = ÷32 output into 50 Ohms.



Channel 1 = 500 MHz clock Channel 2 = ÷32 output into 1M.



Channel 1 = 50 MHz clock 100mv RMS Channel 2 = ÷4 output into 50 Ohms.